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TITLE: INTEGRATED CIRCUIT ON HIGH PERFORMANCE CHIP

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INTEGRATED CIRCUIT ON HIGH PERFORMANCE CHIP

RELATED APPLICATIONS

This application claims priority from French Patent Application No. 0307617 filed June 24, 2003, which is incorporated by reference herein.

BACKGROUND

The present invention relates to the field of integrated circuits, and in particular to that of passive components integrated on die.

In the field of integrated circuits, there is an increasing requirement: to reduce the size taken up by the components, to reduce the fabrication costs, and to introduce new functions.

To achieve these objectives, it is necessary to integrate collectively onto the same analog or digital integrated circuit die an increasing number of components that were previously fabricated separately. There are essentially three categories of such components: circuits called "active" (transistors), components called "passive" (resistors, capacitors, inductors), and, finally, micro-electro-mechanical systems (MEMS) (acoustic filters, radio-frequency switches, variable capacitors).

Passive components and/or MEMS can be integrated independently of transistors, but their monolithic integration with transistors is the most beneficial in terms of compactness and cost. However, this monolithic integration causes a certain number of technological difficulties.

First, the nature of the layers and the treatments necessitated by the fabrication of the passive components are not always readily compatible with fabrication on the active circuits. For example, there exist situations in which the production of a second material after that of a first material in a stack on a silicon wafer necessitates the use of a temperature higher than that above which said first material is degraded unacceptably. This is the case in particular for integrating decoupling capacitors into integrated circuits. These capacitors must store a high electrical charge - the electrical charge is proportional to the capacitance and to the supply voltage, so increasing the

capacitance improves the required performance (it will be remembered that the capacitance is proportional to the dielectric constant and to the electrode area and inversely proportional to the thickness of the dielectric of the capacitor).

Capacitors are conventionally produced on the same wafer as transistors. To reduce production costs, it is naturally desirable to use small capacitors. Obtaining the required capacitances using dielectric materials with a dielectric constant that is very high compared to the usual materials (SiO_2, Si_3N_4, Ta_2O_5, ZrO_2 or Al_2O_3) may then be envisaged.

There exist ferroelectric materials, belonging to the class of perovskites, which have very high dielectric constants (relative constant of several hundred units). Perovskites constitute almost all of the materials investigated for high-capacitance capacitor applications in the required range of dielectric constants (see for example the paper by T. Ayguavives et al. entitled "Physical Properties of (Ba,Sr)TiO_3 Thin Films used for Integrated Capacitors in Microwave Applications", IEEE 2001). The perovskite crystalline phase is usually obtained at temperatures from 600°C to 700°C. However, these temperatures are incompatible with the aluminum- or copper-based interconnection metal of the transistors. Although certain prior art low-temperature processes use a perovskite (see for example the paper by D. Liu et al. entitled "Integrated Thin Film Capacitor Arrays", International Conference on High Density Packaging and MCMs, 1999), they in fact relate to a phase in which the perovskite is not pure or is of mediocre structural or microstructural quality, which means that the dielectric constant is very much lower than that of the same material when annealed at a higher temperature.

The standard methods mentioned hereinabove therefore do not really exploit the advantages of perovskites, because the maximum authorized temperature decreases progressively as and when the process steps are carried out, and the main difficulty results from the fact that the placement of a "hot" process material (the dielectric) occurs after that of a "cold" process material (the interconnection metal).

There is nevertheless known in the art a method for heating the dielectric to a temperature higher than the interconnection metals can withstand. It consists in isolating the dielectric from the interconnection metal by means of a thermal protection layer and then annealing the dielectric using a pulsed laser with sufficiently brief pulses for the temperature of the metal to remain lower than the temperature of the dielectric and to remain acceptable, provided that thermal diffusion is relatively low (see for example the paper by P.P. Donohue et al. entitled "Pulse-Extended Excimer Laser Annealing of Lead Zirconate Titanate Thin Films", proceedings of the 12th International Symposium on Integrated Ferroelectrics, Aachen, Germany, March 2000, published in Integrated Ferroelectrics, vol. 31, pages 285 to 296, 2000). This method is difficult to control, however, because the protective layer remains on the wafer. The protective layer therefore cannot be very thick (it is usually less than 2 μm thick), and it may affect the electrical performance of the devices. The temperature difference between the interconnection metal and the dielectric is therefore limited; in other words, the temperature to which the dielectric may be subjected is limited. Moreover, the stack is subjected to a high thermal gradient during this operation, which can generate a surface temperature that is too high or cause non-homogeneous crystallization of the dielectric or deterioration of materials, such as microcracks, as a result of thermal expansion.

One prior art solution to this temperature problem consists in producing the passive devices incorporating the capacitors on a silicon wafer other than the substrate containing the active components and then connecting the two dies together by wires or by microballs (see for example the paper by R. Heistand et al. entitled "Advances in Passive Integration for C/RC Arrays & Networks with Novel Thin & Thick Film Materials", 36th Nordic IMAPS conference, Helsinki, 1999). These methods have certain drawbacks, however: wires cannot be used to make short connections between capacitor and transistors, and microball connections may be produced on top of a circuit only once; if the capacitors are made of this material, it is no longer possible to add other functions such as switches or surface wave filters, for example.

To avoid these problems, the production temperature is usually limited to about 450°C, which enables integration of the components in the usual metallizations, or above them, in integrated circuits based on aluminum or copper (see for example the paper by S. Jenei et al. entitled "High-Q Inductors and Capacitors on Si Substrate", IEEE 2001, or the paper by Bryan C. Hendrix et al. entitled "Low-Temperature Process for High-Density Thin-Film Integrated Capacitors", International Conference on High-Density Interconnect and Systems Packaging, 2000). Because of this temperature limit, these standard methods are greatly limited in terms of the type of material and the dielectric constants that can be achieved. The required capacitance values are therefore obtained by producing capacitors occupying a large area, which limits the integration possibilities and adds to the cost of the die because of the increased area that is occupied on the silicon wafer.

There is nevertheless known in the art a method for increasing the area of the electrodes without increasing the lateral dimensions of the die (see the paper by F. Roozeboom et al. entitled "High-Value MOS Capacitor Arrays in Ultradeep Trenches in Silicon", published in Microelectronic Engineering, vol. 53, pages 581 to 584, Elsevier Science 2000). This method consists in exploiting the depth of the substrate to integrate metal oxide semiconductor (MOS) decoupling capacitors by excavating an array of deep narrow trenches in the substrate: a dielectric layer and then an electrode layer are disposed around these trenches - the other electrode of the array of capacitors covers the surface of the substrate. However, apart from the difficulty of producing uniform dielectric layers in the trenches, the use of capacitor arrays in trenches makes planar integration of passive components with active components difficult.

More generally, a second difficulty arising from the monolithic integration of passive components or MEMS with transistors is that it is not possible to exploit the vertical dimension to improve the characteristics or the compactness of the passive components.

A third difficulty to which the monolithic integration of passive components or MEMS with transistors gives rise is that the type of substrate

used for the active circuits disturbs the characteristics of the passive components.

For example, the substrates used for CMOS or BICMOS circuits have conductivities of the order of 10 Ω.cm at most. The currents induced in these substrates by the inductors or conductive lines cause high losses and thereby reduce the quality factors of these structures (high inductance, high resonant frequency, low stray capacitance).

A first prior art solution consists in eliminating a portion of the substrate under the areas that are to receive the inductors and conductive lines (see for example US patent 5,539,241). A second prior art solution consists in making the substrate insulative under the areas that are to receive the inductors and conductive lines (see for example the paper by H.-S. Kim et al. entitled "A Porous-Si-based Novel Isolation Technology for Mixed-Signal Integrated Circuits", Symposium on VLSI Technology, 2000). A third solution is disclosed in US patent 6,310,387- the underlying conductive layers are structured by producing a large number of small conductive areas in a checkerboard pattern that are separated from each other by an insulator and are not grounded. These areas serve as shielding because, in operation, low eddy currents are produced therein that prevent the magnetic field penetrating as far as the substrate; these areas are small enough to prevent these eddy currents inducing in the inductors a magnetic flux opposite to the required flux.

However, these various techniques are complex to use, may compromise the robustness of the integrated circuit and make the placement of active components difficult.

Finally, a difficulty raised specifically by the monolithic integration of MEMS with transistors is that it is necessary to add a cover to protect the mechanical components, without interfering with their operation. One prior art solution consists in bonding a silicon wafer of the same diameter as the wafer on which the circuits have been produced (see for example the paper by H. Tilmans et al. entitled "Zero-Level Packaging for MEMS or MST Devices: the IRS Method", mstnews 1/00). This technology is relatively costly because it is necessary to add to the cost of the supplementary substrate the cost of

bonding, the cost of thinning and the cost of local etching to obtain access to the output electrical contacts on the surface of the circuit, and all of this is needed only to provide protection by means of a cover.

BRIEF SUMMARY

To solve most of the difficulties described hereinabove, a first aspect of the invention proposes a method of fabricating a die containing an integrated circuit comprising active components and passive components, said method being distinguished in that it comprises the following steps: a first substrate is produced containing at least one active component of said active components and a second substrate is produced containing "critical" components of said passive components, and the two substrates are bonded by layer transfer. The active components may be transistors, for example.

Passive components are said to be "critical" if their production directly on the substrate containing the active circuits and the metallic interconnections would give rise to a problem; for the reasons explained hereinabove, this may refer to MEMS, for example, and/or high-quality inductors and/or capacitors whose dielectric material is a perovskite.

Certain critical passive components, such as MEMS and/or capacitors, are preferably produced in said second substrate before said bonding of the two substrates.

According to the invention, a second material may in particular be produced on a silicon substrate at a temperature higher than the maximum temperature to which the silicon substrate may be heated because of a first material already present on the wafer. The invention enables this by producing the second material separately from the silicon wafer on which it is to end up and then integrating the second material onto that wafer by layer transfer techniques. In the particular case of decoupling capacitors, the invention enables the dielectric material of the capacitor to be heated to temperatures enabling crystallization in the perovskite phase without any restriction being imposed by the underlying interconnection metal and without having recourse to a thermal protection barrier between the two materials.

The method of the invention also produces conveniently a structure for protecting the MEMS. This is because the MEMS being produced on the surface of the second substrate that is to be transferred onto the first substrate is this first substrate itself (in which an appropriate cavity has been formed beforehand) that serves as a protective structure for the MEMS after bonding the two substrates. This has the advantage that it economizes on the production of a cover as in the prior art.

According to particular features of the invention, dielectric insulation trenches intended to reduce electromagnetic interference between the various components of the future die are further produced during the production of the second substrate.

According to other particular features, non-critical passive components, such as capacitor arrays in trenches are further produced during the production of the second substrate.

Certain other critical passive components are preferably produced in the vicinity of the face of the second substrate opposite the bonding face after said bonding of the two substrates. In the case of inductors, this has the advantage of considerably reducing the effects of the induced currents (energy losses, interference suffered by the active components, etc.), even if the second substrate is conductive, since this places the inductors far from the first substrate.

To reduce further the losses caused by induced currents and to improve the quality factors of the inductors, according to particular features, the inductors will be produced on top of inductive insulation trenches previously formed in the second substrate. A second aspect of the invention also relates to different dies containing integrated circuits.

Thus, first, the invention relates to a die fabricated by any of the methods briefly described above. Second, the invention relates to a die containing an integrated circuit comprising active components and passive components and consisting of a single stack of layers, said die being distinguished in that it includes an interface between two of said layers such that the portion of the die situated on one side of said interface contains at

least one active component of said active components and the other portion of the die contains "critical" components of said passive components. According to particular features, said critical passive components comprise capacitors whose dielectric material is a perovskite and/or MEMS enclosed in cavities situated inside said die.

According to particular features, the die further comprises dielectric insulation trenches. According to other particular features, said integrated circuit further comprises non-critical passive components such as capacitor arrays in trenches.

According to other particular features, said active components are disposed in the vicinity of a first face of the die and said integrated circuit further comprises inductors situated in the vicinity of the face of the die opposite said first face. According to even more particular features, said inductors are situated above inductive insulation trenches.

According to other particular features, said active components are disposed in the vicinity of a first face of the die which further comprises interconnection lines that emerge in the vicinity of the face of the die opposite said first face. The advantages of these dies are essentially the same as those of the corresponding fabrication processes.

Other aspects and advantages of the invention will become apparent on reading the following detailed description of particular embodiments given below by way of non-limiting example.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention can be better understood with reference to the following drawings and description. The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention. Moreover, in the figures, like referenced numerals designate corresponding parts throughout the different views.

Figure 1 shows a first substrate treated by one embodiment of the invention.

Figure 2 shows a second substrate treated by that embodiment of the invention.

Figure 3 shows the assembly obtained after transfer in accordance with the invention of said second substrate 2 onto said first substrate 1.

Figure 4 shows the die obtained by this embodiment of the invention.

Figure 5 is a view to a larger scale of a portion of figure 4.

DETAILED DESCRIPTION

Figure 1 shows a "first" substrate 1 consisting of a wafer of silicon or any other type III-V semiconductor material. The method of the invention begins with the preparation of two substrates 1 and 2 in either order or simultaneously. This first substrate 1 contains active components 3 that have been integrated by any technique known in the art (for example the CMOS or BICMOS technique) and metal interconnections (not shown).

In this embodiment, a thick layer 4 of insulation, for example SiO_2, is deposited and, where appropriate, etched locally (forming cavities 5) in vertical alignment with any Microelectromechanical Systems (MEMS) components on the second substrate. Finally, metallization areas 9 are produced that are subsequently connected to other portions of the die (see below).

Figure 2 represents a wafer forming a "second" substrate 2. In this embodiment, the second substrate 2 has been formed with: dielectric insulating trenches 6, capacitors 7 with a very high dielectric constant, MEMS 8, capacitor arrays 15 in trenches, and inductive insulation trenches 18.

The fabrication of capacitors 7 whose dielectric material is a perovskite will be described in detail. Two embodiments will be described by way of example. In a first embodiment of capacitors 7 whose dielectric material is a perovskite, a second substrate 2 is made of an insulative material, high-resistivity silicon or a semi-insulator such as glass. The following steps are then carried out: a) a layer of silicon oxide SiO_2 is deposited; b) a first electrode is deposited. The first electrode may consist of a plurality of layers of metallic materials, for example, a layer of Ti, RuO_2 or IrO_2, covered with a

layer of platinum; c) using any prior art method (for example the Sol Gel, cathode sputtering, or MOCVD method), the dielectric material is deposited, consisting of a thin layer of a perovskite such as $SrTiO_3$, $Pb(Zr_xTi_{1-x})O_3$ (known as "PZT") or $(Ba_xSr_{1-x})TiO_3$ (known as "BST"); d) the dielectric material is annealed at a high temperature (for example 700°C) to obtain the perovskite phase; e) a second electrode is deposited, which may consist of a plurality of layers of metallic materials, for example a layer of platinum covered with a layer of Ti; and f) a layer of insulation, for example SiO_2, is preferably deposited to encourage subsequent bonding (see below).

Another method of fabricating capacitors 7, whose dielectric material is a perovskite, uses as the second substrate 2 a thick layer of perovskite produced beforehand. In this case, the above steps a) to d) are omitted.

The method of the invention therefore produces, at the required high temperature, capacitors having a dielectric of very high dielectric constant without risk of damaging the active components or the metallic interconnections of the future integrated circuit.

The MEMS components 8 may operate electromechanically or electroacoustically, such as electromechanical switches or acoustic resonators. The MEMS components 8 are produced in a manner that is known in the art by a succession of deposition and etching operations.

The fabrication of capacitor arrays in trenches 15 is described in detail next. The capacitors have electrodes of large area (and therefore also of high capacitance), which are implanted as described in the paper by F. Roozeboom cited above. To be more precise: a) trenches are etched in accordance with predefined patterns and to a depth slightly greater than the future thickness of the substrate after thinning (see below); b) a high-quality dielectric is grown on the faces of each trench. This dielectric must be as thin as possible for the capacitance values of the capacitors 15 to be as high as possible. For example, if the voltage to be applied to the terminals of the capacitors is a few volts, a thickness of dielectric from 10 nm to 50 nm is preferably grown. If the substrate 2 is of silicon, silicon oxide obtained by a thermal effect is advantageously used for this purpose, possibly in

combination with nitriding or deposition of silicon nitride. Dielectrics of higher permittivity may also be used, for example Al_2O_3, HgO_2 or Ta_2O_5 deposited in a manner known in the art; c) the trenches are filled with a highly conductive material to produce one of the plates of the capacitor. Undoped polycrystalline silicon or polycrystalline silicon that is doped in situ may be used for this purpose, for example; and d) localized etching of said highly conductive material is carried out by masking to delimit areas on the surface of the substrate 2 and isolate the plates of the capacitor from the remainder of the semiconductor circuit.

A high-conductivity material (such as silicon) is preferably selected for the substrate 2 because the substrate will constitute one of the plates of the capacitors in trenches. The flanks of the trenches on the substrate side must be strongly doped to render the substrate sufficiently conductive. Finally, an ohmic contact will be produced on the substrate in order to be able to connect one electrode of the capacitors to an electrical circuit.

Alternatively, in the case of integrated circuits that do not include any capacitor arrays in trenches, it is instead preferable to select a low-conductivity material (such as glass) for the second substrate 2 to limit the losses caused by induced currents generated by the inductors (see below).

By making it possible to excavate deep trenches in the second substrate 2, the invention grows electrodes of large area for these capacitors and thereby, for a given substrate lateral area, considerably increases the capacitance value compared to a standard monolithic integration method.

The inductive insulation trenches 18 are produced in accordance with the teaching of US patent 6,310,387 summarized above. As already explained, these trenches 18 contribute to the production of inductors of high quality.

Finally, metallization produces contacts on the plates of the capacitors 7 of very high capacitance value, and on the MEMS 8 and connects them to each other. Metallization areas 10 are also produced that are subsequently connected to other portions of the die by vias formed through the second substrate 2 (see below). Mechanical-chemical polishing is preferably applied

to the upper layer of the resulting wafer to impart to it a roughness encouraging layer transfer by molecular adhesion.

Figure 3 shows the combination obtained after bonding the second substrate 2 onto the first substrate 1 by the method of the invention. The bond between the first substrate 1 and the second substrate 2 is preferably obtained by molecular adhesion or polymer gluing. It is preferable to avoid using a glue layer in order not to increase the total number of layers. However, this bond could also be produced by eutectic or anodic bonding, for example. It may be inconvenient to use soldering and brazing here, however, because of the attendant problems, well known to the person skilled in the art, of wettability, degassing and thermal insulation.

Thus, in the die produced by the method of the invention, the interface at which the two substrates have been bonded delimits two portions of the die. One portion contains at least one active component of the integrated circuit and the other portion contains the critical components of the integrated circuit.

It will be noted in particular that, in this embodiment, the alignment between the MEMS 8 and the cavities 5 is respected. Thus, the fabrication method of the invention protects electromechanical components such as these MEMS 8.

At this stage, to complete the fabrication of the die of the invention, it is necessary to construct the array of interconnections for connecting the electrodes of the capacitors and the underlying array of interconnections of the second substrate 2. It will be noted that here, in the context of the invention, access to buried layers is facilitated, in contrast to prior art monolithic fabrication methods, in which each successive layer may be deposited and immediately etched.

These final steps yield the die 100 shown in figure 4: a) The second substrate 2 is thinned and polished, for example by mechanical-chemical polishing. As explained in patent EP0807970, it is also possible to effect ionic implantation in a plane of the substrate 2 to create microcavities that weaken the substrate and allow subsequent fracture in this plane.

Thinning is continued until it penetrates into the trench structures 6, 15 and 18; a first substrate is produced containing at least one active component of said active components and a second substrate is produced containing "critical" components of said passive components, and the two substrates are bonded by layer transfer; b) the second substrate 2, and then the dielectric layers in vertical alignment therewith are etched locally to uncover the future contacts on the metallization areas 9 and on the metallization areas 10; c) an insulator 11, for example SiO_2, is deposited at low temperature to cover the free surface of the second substrate 2; d) vias 16 (respectively 17) are produced to connect the metallization areas 9 (respectively 10) to the free surface of the insulator 11. In this embodiment the technique disclosed in the paper by M. Tomisaka et al. entitled "Electroplating Cu Fillings for Through-Vias for Three-Dimensional Chip Stacking" (Electronic Components and Technology Conference, 2002) is used. Figure 5 shows this interconnection between the components of the first substrate 1 and the components of the second substrate 2 by means of vias. The insulator 11 is etched first: to produce recessed patterns and holes known as "vias" in the insulator at predetermined locations intended to delimit future conductive lines, and to eliminate the insulator at the bottom of the vias. This etching is followed by conductive metallization of the surface and the inside of the holes formed in the insulator. For this purpose, thin layers of TaN or TiN are deposited, and this continuous base layer is used for electrolytic deposition of thick copper; and e) this copper and said continuous base layer are planarized using techniques known in the art (for example mechanical-chemical polishing) until the copper and the continuous base layer are completely eliminated from the higher areas of the insulator, so as to leave metal only in the recessed patterns produced in the step d) in the trenches of the insulator and in the vertical holes. In this way, vias (16, 17) and inductors 12 on the surface with a so-called "Damascene" structure are obtained (see figure 5). The depth of the recesses and the thickness of the metal are selected to minimize the resistance of this layer.

In a different embodiment, the metallization may be effected, in a manner known in the art, by a tungsten via associated with aluminum lines or areas.

The invention greatly reduces induced current losses, because producing these inductors 12 on the face of the second substrate 2 opposite the bonding face moves these inductors 12 away from the first substrate 1 (which may be a good conductor), and away from the trenches 18 situated under the inductors 12 to eliminate induced currents.

The present invention is not limited to the embodiments described hereinabove. The person skilled in the art will be able to develop diverse variants of the invention without departing from the scope of the appended claims. For example, there are described above embodiments in which the etching of the various layers is effected after transferring the second substrate onto the first. However, it is entirely possible to effect certain etching steps on the first substrate 1 and/or on the second substrate 2 before the transfer step. Also, other elements could naturally be added to the elements constituting the embodiments described above, such as barrier layers or non-stick layers.

Any embodiment of the fabrication method of the invention comprises, as explained above and as shown in the figures, the bonding of the substrates (1) and (2) by layer transfer, i.e., by adhesion of a face of the first substrate (1) to a face of the second substrate (2) over the major portion of their area (known as "full wafer" adhesion).

It will be noted that the die obtained in this way is particularly robust, as it consists of a single stack of layers (compared to prior art devices consisting of portions joined together by soldering or brazing joints or beads). This robustness in particular enables the safe production of cavities (hollow patterns, vias, etc.) in the die during the final fabrication stages, i.e., after bonding the two substrates. As explained above, inductors or interconnections (for example) may therefore be included in the integrated circuit in a manner that is particularly convenient. It will also be noted that, for the same reasons, the die obtained in this way is particularly compact compared to said prior art devices.

While various embodiments of the invention have been described, it will be apparent to those of ordinary skill in the art that many more embodiments and implementations are possible within the scope of the invention. Accordingly, the invention is not to be restricted except in light of the attached claims and their equivalents.